Docket No.: 08211/1200663-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Maria Rosaria Tursi et al.

Patent No.: 7,015,729

Issued: March 21, 2006

For: APPARATUS AND METHOD FOR SAMPLE-AND-HOLD WITH BOOSTED HOLDING SWITCH

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several Patent Office errors which should be corrected.

In the Specification:

First Page Col. 2 (Other Publications), Line 2, Delete "anc" and insert -- and --.

First Page Col. 2 (Other Publications), Line 4, Delete "0.25um" and insert

-- 0.25-um--.

Column 3, Line 7, Delete "sample-and- hold" and insert -- sample-and-hold--.

Column 3, Line 53, Delete "C_{s1}," and insert - - C_{s1} - -.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: June 9, 2006

Respectfully submitted,

By _____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,015,729
APPLICATION NO.	:	10/816,322
ISSUE DATE	:	March 21, 2006
INVENTOR(S)	:	Maria Rosaria Tursi et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

First Page Col. 2 (Other Publications), Line 2, Delete "anc" and insert -- and --.

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PTO/SB/08a/b (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/816,322
Filing Date	March 30, 2004
First Named Inventor	Maria R. Tursi
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	08211/1200663-US1/P05913

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	K. Nagaraj, D. Martin, M. Wolfe, R. Chattopadhyay, S. Pavan, J. Cancio and T.R. Viswanathan, "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-um Digital CMOS Process", IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, pp. 1760-1768, December 2000	
	CB	C. Eichenberger and W. Guggenbuhl, "Dummy Transistor Compensation of Analog MOS Switches", IEEE Journal of Solid-State Circuits, Vol. 24, No. 4, pp. 1143-1146, August 1989	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

{S:\08211\1200663-US1\80008712.DOC [redacted]}	Examiner Signature	Date Considered	

In operation, during a sample phase for sample-and-hold channel 111, sampling switch circuit S_{s1} is closed and switch circuit S_{h1} is open. During the sample phase for sample-and-hold channel 111, sampling capacitor circuit C_{s1} may sample voltage VIN. Similarly, sample-and-hold channel 111 is arranged such that, during a hold phase for sample-and-hold channel 111, sampling switch circuit S_{s1} is open and switch circuit S_{h1} is closed. Also, during the hold phase for sample-and-hold channel 111, switch circuit S_{h1} is arranged to provide signal SH_out1 to first channel 121. First channel 121 may continue processing signal SH_out1 during the subsequent sample phase. Since switch circuit S_{h1} is open, first channel 121 does not receive a new signal until the next hold phase for sample-and-hold channel 111. This way, first channel 121 can use the hold phase for sample-and-hold channel 111 and the subsequent sample phase for sample-and-hold channel 111 to process signal SH_out1 until the next sampled signal needs to be processed by first channel 121.

In a similar manner, sample-and-hold channel 112 is arranged such that, during a sample phase for sample-and-hold channel 112, sampling switch circuit S_{s2} is closed and holding switch circuit S_{h2} is open. During the sample phase for sample-and-hold channel 112, sampling capacitor circuit Cs2 may sample voltage VIN. Also, sample-and-hold channel 112 is arranged such that, during a hold phase for sample-and-hold channel 112, sampling switch circuit S_{s2} is open and holding switch circuit S_{h2} is closed. As described with regard to switch circuit S_{h1} above, second channel 122 can use the hold phase for the sample-and-hold channel 112 and the subsequent sample phase for sample-and-hold channel 112 to process signal SH_out2 until the next sample needs to be processed by second channel 122.

In one embodiment, by pipelining sample-and-hold circuit 102 in two in the manner described, the speed of sample-and-hold circuit 102 is substantially doubled, without substantially decreasing the processing time allowed for processing circuit 120. In other embodiments, sample-and-hold circuit 102 may be pipelined by more than two.

Processing circuit 120 may be interleaved such that first channel 121 and second channel 122 are substantially similar.

In one embodiment, signals VIN, SH_out1 and SH_out2 are all single-ended signals. In other embodiments, one or more of signal VIN, SH_out1 and SH_out2 are

differential signals. In another embodiment, although not shown, circuit 100 may be arranged to operate in single-ended mode if signal SE (not shown) is asserted, and to operate in differential mode if signal SE is not asserted.

FIGURE 2 illustrates a block diagram of an embodiment of circuit 200 in which the sample-and-hold circuit includes buffer circuits, and the processing circuit is an ADC circuit. Components in circuit 200 may operate in a substantially similar manner to similarly-named components in circuit 100, and may operate in a different manner in some ways. Processing circuit 220 is an interleaved ADC circuit that includes ADC bank 221 and ADC bank 222. Sample-and-hold circuit 202 further includes buffer circuits 236, 238, and 230.

In operation, buffer circuit 230 may provide signal VIN_buf from signal VIN. Buffer circuit 230 may prevent kickback noise created by the switching operation and by transient currents drawn by sampling capacitor circuits C_{s1} and C_{s2}. Similarly, buffer circuits 236 and 238 may help stop any constant or transient current drawn by processing circuit 220 that might otherwise corrupt the voltage stored in sampling capacitor circuits C_{s1} and C_{s2} respectively.

Switch circuits S_{s1} and S_{h2} are arranged to be closed if signal phi1 is high, and arranged to be open if signal phi1 is low. Conversely, switch circuits S_{s2} and S_{h1} are arranged to be closed if signal phi2 is high, and arranged to be open if signal phi2 is low. During the hold phase for switch circuit S_{h1}, the relatively large input capacitance associated with ADC bank 221 is not coupled to sampling capacitor circuit C_{s1}. Also, a break-before-make scheme may be implemented so that a short delay occurs between the time that sampling switch circuit S_{s1} turns off and the time that hold switch circuit S_{h1} turns on, and so that another short delay occurs between the time that hold switch circuit S_{h1} turns off and the time that sampling switch circuit S_{s1} turns on. Additionally, although not shown in FIGURE 2, signals phi1 and phi2 are provided from one of more clock signals CLKs.

Sample-and-hold channel 212 operates in a substantially similar manner as sample-and-hold channel 211, except than sample-and-hold channel 212 is sampling when sample-and-hold channel 211 is holding, and vice versa.